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UNITED STATES PATENT APPLICATION

FOR

A VERY LOW CURRENT OSCILLATOR WITH VARIABLE DUTY CYCLE

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5 A VERY LOW CURRENT OSCILLATOR WITH VARIABLE DUTY CYCLE

TECHNICAL FIELD

10 The present invention relates to the field of low-power integrated circuits. More particularly, the present invention relates to low current oscillator circuits.

BACKGROUND ART

15 Minimizing power consumption is critical in extending operating time in portable or battery power devices. The lower the power consumption of the circuit elements of, for example, a handheld cell phone, the longer the handheld cell phone can provide its functionality to the user. Accordingly, circuit elements of a given device are designed for minimal power consumption.

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Low power consumption constraints generally apply to all elements of an integrated circuit device, such as, for example, processors, output drivers, displays, etc. The circuit elements are designed to interact and function with each other, and must adequately
25 perform their required function while remaining within the desired

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power consumption constraints. Oscillator circuits comprise one of the most fundamental circuit elements of electronic devices.

Oscillators are used to produce a wide variety of periodic signals (e.g., clock signals, etc.). Many of the components of an integrated circuit device rely on clock signals generated by oscillator circuits to produce their functionality. For example, modern analog to digital converters (ADCs) function by using low jitter external clock source. ADCs are specified to operate with a clock signal having a duty cycle that varies across a specified range.

Similarly, most signal sampling mechanisms common to data communication applications rely on high-quality clock signals to sample incoming data. It is becoming increasingly common for such sampling mechanisms to function on both the rising edge and the falling edge of a clock signal, thereby making duty cycle control an important factor. As is well known, a clock signal's duty cycle refers to a ratio of one clock phase width to the entire clock period.

A problem exists, however, with prior art oscillator circuits. As described above, high-quality clock signals are critical to functioning of many different functional blocks of an integrated circuit device. To produce such high-quality clock signals, and to provide a precise adjustable duty cycle, prior art oscillator circuits include a large number of transistors, current sources, and other circuit elements. These elements tend to increase power consumption, thereby reducing battery life of a handheld device. Additionally, a large number of circuit elements increase the amount of silicon area dedicated to the oscillator circuit, thereby increasing the cost of the overall device.

Prior art Figure 1 shows a diagram of a typical prior art oscillator circuit 100. The prior art oscillator circuit 100 includes two amplifiers 151-152. The oscillation is driven primarily from the action of the
5 amplifiers 151-152, which function as comparators. The output of the comparators 151-152 are respectively coupled to the NAND gates 121-122 as shown. The NAND gates 121-122 are coupled in a feedback loop as depicted, which oscillates between a high-value and a low value. The output of the oscillator circuit 100 is derived from the output of the
10 inverter 123.

The oscillator circuit 100 includes the current sources 101-105 as shown. The high voltage level and the low voltage level between which the oscillator circuit 100 oscillates is set by the voltages V_1 and V_2 as
15 derived from the current from the current source 101 flowing through a resistor 111 and a resistor 112. The voltages V_1 and V_2 are coupled to the positive input of comparator 151 and the negative input of comparator 152 as shown. In this manner, the current source 101 (e.g., I_1) creates the voltages V_1 and V_2 .

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The current source 102 and the current source 103 bias the comparators 151-152 as shown. The current source 104 and the current source 105 are used to charge and discharge the capacitor C_1 , and thereby produce the output signal at node 130. As shown in prior
25 art Figure 1, the current source 104 charges the capacitor C_1 to the voltage V_2 and the current source 105 discharges the capacitor C_1 to the voltage V_1 .

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One problem with prior art oscillator circuit 100 is that it consumes too much power. As shown in prior art figure 1, the oscillator circuit 100 requires five current sources 101-105 in order to function. Each of these current sources represents a power consuming element.

- 5 Another problem is the fact that the prior art oscillator circuit 100 requires two comparators 151-152, which both consume power.

Yet another problem with the prior art oscillator circuit 100 is the fact that it requires a constant current flow, and thus a constant
10 power drain, from the current source 101 across the resistor 111 and the resistor 112. These current flows are required in order to create voltages V_1 and V_2 .

Thus, what is required is a solution for implementing a very low
15 power consumption oscillator circuit for an integrated circuit device. The required solution should provide an adjustable duty cycle that can be set in accordance with the needs of a given application. Additionally, the required solution should require fewer circuit elements in comparison to prior art oscillator circuit implementations.

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SUMMARY OF THE INVENTION

Embodiments of the present invention provide a solution for implementing a very low power consumption oscillator circuit for an integrated circuit device. Embodiments of the present invention
5 provide an adjustable duty cycle that can be set in accordance with the needs of a given application. Additionally, the embodiments of the present invention require fewer circuit elements in comparison to prior art oscillator circuit implementations.

10 In one embodiment, the present invention is implemented as a low current oscillator circuit comprising a comparator for driving an output signal. A first capacitor chain is coupled to the comparator. The first capacitor chain is configured for setting a first input voltage of the comparator. A second capacitor chain is also coupled to the
15 comparator. The second capacitor chain is configured for setting a second input voltage of the comparator, wherein the first capacitor chain and the second capacitor chain determine a first voltage level and a second voltage level of oscillation of the comparator (e.g., the high level and the low level of the voltage swings of the output of the
20 comparator). The first capacitor chain and the second capacitor chain are both free of DC current flow, thereby providing for a very low power consumption of the oscillator circuit. In one embodiment, the ratios between the capacitors of the capacitor chains determine the first and second voltage levels of oscillation. In one embodiment, a switch circuit
25 is coupled to the comparator to set the duty cycle of the oscillation of the comparator.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements.

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Prior art Figure 1 shows a diagram of a typical prior art oscillator circuit.

Figure 2 shows a diagram of a very low current oscillator circuit
10 in accordance with one embodiment of the present invention.

Figure 3 shows a first graph and a second graph depicting signals of the oscillator circuit in accordance with one embodiment of the present invention.

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Figure 4 shows a graph of the overall power consumption of the oscillator circuit in accordance with one embodiment of the present invention.

20 Figure 5 shows a schematic diagram of an oscillator circuit in accordance with one embodiment of the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with
5 the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the
10 following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be understood by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known
15 methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Embodiments of the present invention provide a solution for
20 implementing a very low power consumption oscillator circuit for an integrated circuit device. Embodiments of the present invention provide an adjustable duty cycle that can be set in accordance with the needs of a given application. Additionally, the embodiments of the present invention require fewer circuit elements in comparison to prior
25 art oscillator circuit implementations. Embodiments of the present invention and their benefits are further described below.

Figure 2 shows a diagram of a very low current oscillator circuit
200 in accordance with one embodiment of the present invention. As

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illustrated in Figure 2, the oscillator circuit 200 includes a single comparator 251. The oscillator circuit 200 also includes a first current source 201 and a second current source 202.

5 The oscillator circuit 200 embodiment is configured as an ultra low current oscillator circuit. The comparator 251 is configured for driving an output signal, which is taken at node 230. The oscillator circuit 200 includes two capacitor chains for setting the voltage levels of the oscillation. The resistors R_1 and R_2 and the capacitors C_1 and C_2
10 comprise the first capacitor chain. Similarly, the resistors R_3 and R_4 and the capacitors C_3 and C_4 comprise the second capacitor chain, as shown.

 In the present embodiment, the voltage levels of oscillation are
15 set by the two capacitor chains. As shown in Figure 1, the comparator 251 has three inputs 252, 253 and 254. Two of these inputs (e.g., 253 and 254) are used to set the levels of the oscillation (e.g., the low voltage level of the oscillation and the high voltage level of the oscillation). In the present embodiment, the input 253 is coupled to V_1
20 of the first capacitor chain and the input 254 is coupled to V_2 of the second capacitor chain. The V_1 and V_2 voltages are created by the ratios of the capacitors of the respective chains. For example, in the oscillator circuit 200 embodiment as shown, the V_1 voltage is determined by the expression $V_1 = C_1 / (C_1 + C_2)$ and the V_2 voltage is determined by the
25 expression $V_2 = C_3 / (C_3 + C_4)$.

 Thus, in contrast to prior art oscillator circuits where a current from a current source must flow across resistors in order to make the input voltages, the V_1 and V_2 voltages are created by the first and

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second capacitor chains that are completely free of DC current flow. In this manner, the oscillator circuit 200 embodiment of the present invention completely eliminates a current flow requirement for setting input voltages for the comparator 251. This aspect greatly reduces the current flow within the oscillator circuit 200 embodiment, thereby greatly reducing the power consumption.

Referring still to Figure 2, the oscillator circuit 200 includes a switch circuit comprising a capacitor C_A and a switch ϕ as shown. The switch circuit functions by initiating the oscillation in the comparator 251. A current source 201 is connected to the capacitor C_A and the switch ϕ . In the present embodiment, the switch circuit functions by setting the duty cycle of the oscillator circuit 200. The node 235 between the current source 201 and a switch circuit is coupled to the input 252 of the comparator 251.

The current source 201 (e.g., I_1) functions by charging the capacitor C_A to the voltage V_2 (e.g., the high voltage level). The switch ϕ functions by discharging the capacitor C_A to the voltage V_1 (e.g., the low voltage level). The configuration of the switch ϕ and the capacitor C_A determines the duty cycle of the output signal (e.g., the signal from output node 230). This duty cycle can be adjusted by adjusting switch ϕ and the capacitor C_A (e.g., in accordance with the requirements of the overall device or system application). A DC current path to ground for the current source 201 exists only when the switch ϕ is closed.

In the oscillator circuit 200 embodiment, the output of the comparator 251 is coupled to a feedback circuit comprising the transistors 211-214 as shown. The feedback circuit functions by

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driving the switching action of the switch ϕ . An output of the oscillator circuit 200 is taken from the node 230.

Depending upon the overall system in which the oscillator 200 is included, the output taken from node 230 can be shaped by additional external circuit elements (not shown). For example, external filtering elements can be coupled to the output in order to smooth the output into, for example, a sine wave. External filtering elements can be coupled to the output to shape the output into a sawtooth wave, or the like. In this manner, the oscillator 200 can provide a wide variety of different periodic signals used in electronic devices.

It should be noted that the oscillator circuit 200 embodiment of the present invention includes only one comparator (e.g., comparator 251), in comparison to prior art oscillator circuit implementations which included two or more comparators. The single comparator 251 only requires a single current source 202 (e.g., I_2), as supposed to the two or more current sources required in prior art oscillator circuit implementations. This aspect further reduces power consumption of the oscillator circuit 200 in comparison to the prior art.

It should also be noted that the oscillator circuit 200 embodiment of the present invention has a low component count in comparison to prior art oscillator circuit implementations. For example, by reducing the number of included comparators (e.g., to one) and by reducing the number of current sources, the component count, and thus the silicon area required to manufacture the oscillator circuit 200, is reduced. The reduced silicon area results in a corresponding reduction in cost.

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These aspects enable the oscillator circuit 200 embodiment of the present invention to implement a very low power consumption oscillator circuit for an integrated circuit device. The low power consumption benefits are provided while enabling duty cycle
5 adjustment and oscillation voltage level adjustment. These features are provided while also reducing manufacturing costs in comparison to prior art.

Figure 3 shows a graph 301 and a graph 302 depicting signals of
10 the oscillator circuit 200 in accordance with one embodiment of the present invention. The horizontal axis of both the graphs 301 and 302 represents time. The vertical axis of the graphs 301 and 302 represents voltage, in the scale shown. The graph 301 shows the voltage at the node 235 of the oscillator circuit 200, as the capacitor C_A
15 charges over time from the current source 201 and is discharged by the switch ϕ . The graph 302 shows the square wave output at node 230. Both graphs 301-302 are shown beginning from an initial power on.

Figure 4 shows a graph of the overall power consumption of the
20 oscillator circuit 200 in accordance with one embodiment of the present invention. As shown in Figure 4, during normal operation, the oscillator circuit 200 draws a constant, very low amount of current. In this embodiment, the oscillator circuit 200 draws approximately 50.248 nano-Amps.

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Figure 5 shows a schematic diagram 500 of an oscillator circuit in accordance with one embodiment of the present invention. The diagram 500 of Figure 5 shows a more detailed illustration of oscillator circuit 200 of Figure 2. The oscillator circuit of the diagram 500

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functions in substantially the same manner as the oscillator circuit 200 described in the discussion Figure 2 above.

5 The correspondence between the schematic diagram 500 and the oscillator circuit 200 of Figure 2 is now described. In the diagram 500 illustration, the capacitor 501 corresponds to capacitor C_A . The transistors 502 correspond to the switch ϕ . The node 503 corresponds to the voltage level V_1 and the node 504 corresponds to the voltage level V_2 . The capacitor 505 corresponds to the capacitor C_1 . The resistor 506
10 and the resistor 507 correspond to the resistors R_1 and R_3 . The capacitor 508 and capacitor 509 correspond to capacitors C_3 and C_4 . Capacitor 510 corresponds to the capacitor C_2 . The resistors 511 and 512 correspond to the resistors R_2 and R_4 . The transistors 513-516 correspond to the transistors 211-214. The output 520 corresponds to
15 the output node 230.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the
20 invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order best to explain the principles of the invention and its practical application, thereby to enable others skilled in the art best to utilize the invention and various embodiments with
25 various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.